# FET HAVING EPITAXIAL SILICON GROWTH

## RELATED APPLICATIONS

**[0001]** This application is a divisional of United States Patent Application Serial No. 10/073,723 filed February 11, 2002 and titled, "FET HAVING EPITAXIAL SILICON GROWTH" (allowed), which application is commonly assigned and incorporated herein by reference. The present invention is related to United States Patent Application Serial No. 09/713,844 to Abbott et al., titled "METHOD OF FORMING A FIELD EFFECT TRANSISTOR," filed November 15, 2000, issued as US 6,599,789 on July 29, 2003, which is commonly assigned and incorporated herein by reference.

## TECHNICAL FIELD OF THE INVENTION

**[0002]** The present invention relates generally to integrated circuit devices, and in particular to the use of epitaxial silicon growth in a field-effect transistor to reduce source/drain junction leakage.

## BACKGROUND OF THE INVENTION

**[0003]** Semiconductor processors continue to strive to reduce the size of individual electrical components, thereby enabling smaller and denser integrated circuitry. One typical device is a field-effect transistor. Such typically includes opposing semiconductive source/drain regions of one conductivity type having a semiconductive channel region of opposite conductivity type therebetween. A gate construction is received over the channel region. Current can be caused to flow between the source/drain regions through the channel region by applying a suitable voltage to the gate.

**[0004]** The channel region is in some cases composed of background doped bulk semiconductive substrate or well material, which is also received immediately beneath the opposite type doped source/drain regions. This results in a parasitic capacitance developing between the bulk substrate/well and the source/drain regions. This can

adversely affect speed and device operation, and becomes an increasingly adverse factor as device dimensions continue to decrease.

**[0005]** Field-effect transistors have been described having channel regions formed separately from the source/drain regions. Such separate formation can result in a grain boundary between the source/drain regions and the channel region, which can produce a junction leakage problem when the grain boundary crosses the source/drain junction.

**[0006]** For the reasons stated above, and for other reasons stated below that will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternative methods for producing field-effect transistors, and their resulting devices.

## SUMMARY

**[0007]** US 6,599,789 cited above includes a method of forming a field-effect transistor (FET) including forming a channel region within a bulk semiconductive material of a semiconductor substrate. Source/drain regions are formed on opposing sides of the channel region. A dielectric region is formed within the bulk semiconductive material proximately beneath at least one of the source/drain regions. The various embodiments described herein can reduce the potential for junction leakage in a FET of the type described in US 6,599,789 by moving a grain boundary of a material interface away from the channel region of the FET. The grain boundary is moved by utilizing an epitaxial silicon growth on exposed portions of the bulk semiconductive material of the semiconductor substrate.

**[0008]** For one embodiment the invention provides a field-effect transistor that has a channel region in a bulk semiconductor substrate, a first source/drain region on a first side of the channel region, a second source/drain region on a second side of the channel region, and an extension of epitaxial monocrystalline material formed on the bulk semiconductor substrate so as to extend away from each side of the channel region.

**[0009]** For another embodiment, the invention provides a field-effect transistor (FET). The FET includes a channel region in a bulk semiconductor substrate, a first source/drain

region on a first side of the channel region, a second source/drain region on a second side of the channel region, an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region, a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region, and a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region.

**[0010]** For another embodiment, the invention provides a FET. The FET includes a channel region in a monocrystalline silicon substrate, a first source/drain region on a first side of the channel region, a second source/drain region on a second side of the channel region, epitaxial silicon formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region, and a gate overlying the channel region. For a further embodiment, the source/drain regions are polycrystalline silicon.

**[0011]** Further embodiments of the invention include apparatus of varying scope.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0012]** Figures 1A-1J are sectional views of the fabrication of a field-effect transistor in accordance with an embodiment of the invention.

**[0013]** Figure 2 is a planar view of a FET produced in accordance with a fabrication process described with reference to Figures 1A-1J.

**[0014]** Figure 3 is a schematic of a portion of a memory array in accordance with an embodiment of the invention.

**[0015]** Figure 4 is a simplified block diagram of an integrated circuit memory device in accordance with an embodiment of the invention.

## DETAILED DESCRIPTION

**[0016]** In the following detailed description of the present embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These

embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that process, electrical or mechanical changes may be made without departing from the scope of the present invention. The terms wafer or substrate used in the following description include any base semiconductor structure. Examples include silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and the terms wafer and substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

**[0017]** Figures 1A-1J depict fabrication of a field-effect transistor (FET) in accordance with an embodiment of the invention. Referring initially to Figure 1A, a semiconductor substrate is indicated generally with reference 10.

**[0018]** Substrate 10 comprises a bulk semiconductor substrate 12. For one embodiment, the bulk semiconductor substrate 12 is a monocrystalline material, such as monocrystalline silicon lightly doped with p-type material. In the context of this document, the term "bulk" also includes doped well regions within such substrates. Bulk semiconductor substrate 12 comprises a channel region 14 which is shown as being masked by a pad oxide layer 13 and a patterned block of masking material 16. For an exemplary 0.15 micron transistor gate width, an exemplary thickness for layer 13 is 100 Angstroms. An exemplary preferred material for mask 16 is silicon nitride deposited to an exemplary thickness of 900 Angstroms. An example width is 0.25 micron. In the illustrated embodiment, masking material 16 extends laterally beyond the lateral confines of channel region 14. Such provides but one example of forming a channel region within bulk semiconductive material of a semiconductor substrate, and of masking the same.

**[0019]** Referring to Figure 1B, at least one trench is formed into the bulk semiconductor substrate on at least one side of the channel region received within the bulk semiconductor substrate. Preferably and as shown, two trenches 18, 19 are formed into bulk semiconductor substrate 12 on opposing sides of masked channel region 14. Such preferably occurs by any existing or yet-to-be developed substantially anisotropic etching technique. An exemplary preferred depth for the trench etching is 1700 Angstroms.

**[0020]** Referring to Figure 1C, a dielectric, or insulative, material 20 is deposited over masking material 16 and within and overfilling trenches 18 and 19. Exemplary and preferred processing includes sidewall oxidation either before or after deposition of layer 20. For a further embodiment, the sidewall oxidation may be performed prior to formation of layer 16. For one embodiment, the material for layer 20 is high-density plasma deposited oxide. The dielectric material is preferably initially deposited to overfill the trenches and then subsequently planarized at least to masking material 16 to provide the construction as illustrated in Figure 1C. Example planarizing techniques include chemical-mechanical polishing (CMP) and resist etch-back.

**[0021]** Referring to Figure 1D, portions of dielectric material 20 are removed from within trenches 18 and 19 effective to form at least one and preferably two as shown, source/drain voids 22 and 24 on the respective sides of channel region 14. Such removal as shown is also preferably effective to expose bulk semiconductive material 12. An example preferred depth of voids 22 and 24 within dielectric material 20 is 1500-2000 Angstroms, or a depth sufficient to expose approximately 500-1000 Angstroms of the bulk semiconductive material 12. For one embodiment, the removal technique is a timed anisotropic etch, and with a photolithographic patterned mask being received over the non-etched portions of layer 20. In the illustrated embodiment, such effectively defines the outlines of the source/drains of the FETs being formed. Preferably and as shown, such removing forms an outer surface of dielectric material 20 to be planar at the base of such voids 22 and 24.

**[0022]** Referring to Figure 1E, an epitaxial silicon growth, or deposition, is performed. Epitaxial silicon growth will be selective to portions of the monocrystalline silicon 12

exposed by voids 22 and 24. The epitaxial silicon will grow both horizontally and vertically from the exposed portions of the monocrystalline silicon 12. Such selective growth will produce the extensions of monocrystalline silicon 23 and 25 in voids 22 and 24, respectively. The extensions of monocrystalline silicon 23 and 25 will move the grain boundary away from the channel region 14, thus facilitating a reduction in potential source/drain junction leakage of the final FET.

**[0023]** Epitaxial deposition of silicon is a chemical vapor deposition (CVD) process used to produce a layer of single crystal material upon a surface of a single crystal substrate. Silicon precursors are transported to, and adsorbed on, the surface of the substrate 10. Common silicon precursors for the production of epitaxial silicon as the single crystal material include silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$), dichlorosilane ($SiH_2Cl_2$) and silane ($SiH_4$). The chemical reaction to produce monocrystalline silicon proceeds preferentially on exposed monocrystalline silicon where nucleation is favored, with the newly formed silicon providing an advancing reaction interface and new nucleation sites.

**[0024]** The process of epitaxial silicon growth is well understood in the art. Typical deposition temperatures range from about 600°C to about 1250°C. Depth of the epitaxial growth is typically controlled through reaction time, or time that the substrate 10 is exposed to the reactant gases and their reaction conditions. Typical reaction times may range from about 1 minute to about 15 minutes or more, depending upon the desired depth. For one embodiment, the extensions of monocrystalline silicon 23 and 25 have a maximum depth of approximately 300 Angstroms to 3000 Angstroms or more. For a further embodiment, the extensions of monocrystalline silicon 23 and 25 have a maximum depth of approximately 500 Angstroms to 1500 Angstroms. For a still further embodiment, the extensions of monocrystalline silicon 23 and 25 have a maximum depth of approximately 1000 Angstroms. For another embodiment, the epitaxial silicon growth may be carried out to fill the voids 22 and 24 with monocrystalline silicon.

**[0025]** Selective epitaxial deposition occurs when silicon atoms having high surface mobility are deposited from the silicon source or precursor. These silicon atoms migrate to

sites on the single crystal material where nucleation is favored. Others have observed that silicon mobility is enhanced by the presence of halides in the reaction gases. Other factors recognized to enhance the selective nature of the silicon deposition include reduced reaction pressure, increased reaction temperature and decreased mole fraction of silicon in the reaction gases. Some polysilicon growth may occur concurrently with the epitaxial growth due to reactions occurring on non-monocrystalline surfaces, e.g., exposed surfaces of the dielectric material 20. However, epitaxial silicon growth on the exposed portions of the monocrystalline silicon 12 should be the dominant reaction.

**[0026]** For one embodiment, the epitaxial silicon growth is undoped monocrystalline silicon. For another embodiment, the epitaxial silicon growth is doped monocrystalline silicon. Doping of the epitaxial silicon growth can be used to alter the conductive properties of the resulting monocrystalline silicon, to reduce the temperature of formation or to otherwise alter the properties of the resulting material. The dopants, or impurities, are added to the reaction gases during the epitaxial silicon growth. Doping epitaxial growth is typically carried out by adding hydrides of the dopant materials to the reaction gases. For example, diborane ($B_2H_6$) may be added to the reaction gases to form a boron-doped monocrystalline silicon. For one embodiment, the epitaxial silicon growth is doped with germanium (Ge). For a further embodiment, the germanium doping is carried out using germanium tetrahydride ($GeH_4$). For a still further embodiment, the epitaxial silicon growth is a growth of a silicon-germanium ($Si_xGe_{1-x}$) alloy. Silicon-germanium alloy can be grown epitaxially on silicon. For one embodiment, the silicon-germanium alloy contains approximately 20 at% germanium or more, e.g., $0 <= x <= 0.8$. For a further embodiment, the silicon-germanium alloy further contains no more than approximately 50 at% germanium, e.g., $0.5 <= x <= 0.8$.

**[0027]** Referring to Figure 1F, source/drain semiconductive material 26 is formed within voids 22 and 24. For one embodiment, the material 26 is polycrystalline material. For one embodiment, the material is polycrystalline silicon, preferably *in situ* conductively doped with a conductivity enhancing impurity during a chemical vapor deposition. The conductivity type for the source/drain material 26 is chosen to be a type opposite that of

the bulk semiconductor substrate 12. For a p-type bulk semiconductor substrate 12, an n-type impurity would be used for the source/drain material 26. The source/drain material 26 preferably covers and physically contacts the extensions of monocrystalline silicon 23 and 25.

**[0028]** Referring to Figure 1G, deposited semiconductive material 26 is planarized at least to a level of masking material 16. Example and preferred techniques include CMP and resist etch back.

**[0029]** Referring to Figure 1H, channel region 14 is unmasked preferably by etching away all of the masking material 16 and all of pad oxide layer 13. Further preferably as shown, some and only some of semiconductive material 26 is etched from the substrate. Such might occur in one or more etching steps depending on the chemistry utilized and the desires of the processor, as readily determinable by the artisan. By way of example only, an example etch chemistry that will etch polysilicon and silicon nitride in a substantially nonselective manner includes plasma $CF_4$, $CH_2F_2$ and He. In the subject example, the preferred amount of semiconductive material left is 900 Angstroms thick. Such provides but one example of forming source/drain regions 30 and 32 on opposing sides of channel region 14. The upper surface of channel region 14 in Figure 1H is preferably approximately 200 Angstroms beneath the upper surfaces of regions 30 and 32, which are also preferably substantially planar. The resulting step between the upper surface of the dielectric material 20 and the upper surfaces of regions 30 and 32 is preferably reduced, if necessary, to between approximately 200-300 Angstroms. Such can be accomplished, for example, with a simple HF clean.

**[0030]** Referring to Figure 1I, a gate 34 is formed over channel region 14. Preferably as shown, a gate dielectric layer 36, for example silicon dioxide, is first formed over channel region 14. A gate stack is then formed over channel region 14. For one embodiment, the gate stack includes a conductively doped polysilicon layer 38 and a conductive silicide layer 40 (for example $WSi_x$) and a nitride capping layer 42. Thereafter, at least one pocket implanting is conducted to provide at least one pocket implant region intermediate source/drain semiconductive material 26 and channel region 14. In the

illustrated and preferred example, exemplary pocket implants include source/drain extension (SDE) implant regions 44 having a thickness of approximately 500 Angstroms, and halo implant regions 46 provided therebeneath having an approximate thickness of 500 Angstroms and to extend below source/drain regions 30 and 32. Insulative spacers are subsequently added as shown. Rapid thermal processing is preferably conducted at some point, as is conventional.

**[0031]** Referring to Figure 1J, subsequent exemplary processing is illustrated. Depicted is the provision and planarizing of a dielectric layer 48, for example borophosphosilicate glass (BPSG). Contact openings have been formed therethrough and plugged with conductive material to form source/drain contacts 50. Figure 2 is a planar view of a FET produced in accordance with a fabrication process described with reference to Figures 1A-1J. Field-effect transistors of the type described herein may be used in a variety of integrated circuit devices. Some examples include memory devices, microprocessors, digital signal processors (DSP) and more.

**[0032]** Figure 3 is a schematic of a portion of a memory array 300 containing field-effect transistors as described herein. The memory array 300 includes a number of memory cells 302 arranged generally in rows and columns. Typical memory arrays 300 contain millions of these memory cells 302. Each memory cell 302 includes an access transistor 304, with the gate of each access transistor 304 coupled to a word line 310. The access transistor 304 is a field-effect transistor in accordance with an embodiment of the invention.

**[0033]** A first source/drain region of an access transistor 304 is coupled to a bit line 312 and a second source/drain region of the access transistor 304 is coupled to a capacitor 306. The data value of the memory cell 304 is stored as a charge on the capacitor 306 and the data value is sensed by charge sharing with the associated bit line 312 and detecting the change to the bit-line potential as a result of the charge sharing. A grouping of memory cells 302 coupled to the same word line 310 are typically referred to as a row of memory cells. Likewise, a grouping of memory cells 302 coupled to the same bit line 312 are typically referred to as a column of memory cells.

**[0034]** Figure 4 is a simplified block diagram of an integrated circuit memory device 400 as a dynamic random access memory (DRAM) device in accordance with an embodiment of the invention. The memory device 400 includes an array of memory cells 402, an address decoder 404, row access circuitry 406, column access circuitry 408, control circuitry 410, and Input/Output (I/O) circuitry 412. The memory array 402 contains memory cells having an access transistor coupled between a bit line and a capacitor.

**[0035]** The memory device 400 can be coupled to a processor 414 or other memory controller for accessing the memory array 402. The memory device 400 coupled to a processor 414 forms part of an electronic system. Some examples of electronic systems include personal computers, peripheral devices, wireless devices, digital cameras, personal digital assistants (PDAs) and audio recorders.

**[0036]** The memory device 400 receives control signals across control lines 416 from the processor 414 to control access to the memory array 402. Access to the memory array 402 is directed to one or more target memory cells in response to address signals received across address lines 418. Once accessed in response to the control signals and the address signals, data is written to or read from the memory cells across DQ lines 420.

**[0037]** The memory cells of the memory array 402 are generally arranged in rows and columns with a memory cell located at each intersection of a bit line and a word line. Those memory cells coupled to a single word line are generally referred to as a row of memory cells while those memory cells coupled to a single bit line are generally referred to as a column of memory cells.

**[0038]** It will be understood that the above description of a DRAM is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a DRAM. Further, the invention is equally applicable to a variety of sizes and types of memory circuits known in the art and is not intended to be limited to the DRAM described above.

**[0039]** As recognized by those skilled in the art, memory devices of the type described herein are generally fabricated as an integrated circuit containing a variety of

semiconductor devices. The integrated circuit is supported by a substrate. Integrated circuits are typically repeated multiple times on each substrate. The substrate is further processed to separate the integrated circuits into dies as is well known in the art.

**[0040]** The foregoing figures were used to aid the understanding of the accompanying text. However, the figures are not drawn to scale and relative sizing of individual features and layers are not necessarily indicative of the relative dimensions of such individual features or layers in application. Accordingly, the drawings are not to be used for dimensional characterization.

**[0041]** Although dimensional characteristics were provided herein for information purposes, it is recognized that there is a continuing drive to reduce integrated circuit device dimensions for increased performance and reduced fabrication costs. In addition, the concepts described herein are not fundamentally limited by absolute dimensions. Accordingly, improvements in fabrication and sensing technologies are expected to facilitate reduced dimensional characteristics of the FET devices described herein, particularly as they relate to layer thickness and width.

## CONCLUSION

**[0042]** Field-effect transistors, and methods of their fabrication, have been described having channel regions formed separately from their source/drain regions and having monocrystalline silicon interposed between the channel regions and the source/drain regions. The monocrystalline silicon interposed between the channel regions and the source/drain regions may be formed through an epitaxial silicon growth as extensions from the channel region. These extensions of epitaxial silicon serve to move the grain boundary of the source/drain regions away from the channel regions. Moving the grain boundary can reduce the likelihood of source/drain junction leakage.

**[0043]** Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the

art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.